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EXAMINER	
NGUYEN, THAN VINH	

ART UNIT	PAPER NUMBER
2187	

DATE MAILED: 05/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/615,326	KLEIN, DEAN A.	
	Examiner	Art Unit	
	Than Nguyen	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 March 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11,13-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11,13-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This is a response to the amendment, filed 3/10/05.

2. Claims 1-11,13-21 are pending. Claims 13-21 are newly added.

3. In view of the amendment to the specification, the previous objection to the specification, the previous objection is withdrawn.

4. In response to the amendment to claim 4,10, the previous 35 USC 112 rejection to these claims are withdrawn.

Response to Arguments/Amendment

5. Applicant's amendment introduces new limitations not considered previously. The new limitations are addressed below.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1,3,4,5,7,8,10,11,13-21 are rejected under 35 U.S.C. 102(b/e) as being anticipated by Baba (US 5,303,192) OR Wiggers (US 6,011,710).

As to claim 1,5:

8. Baba teaches a semiconductor memory device and its connection. Baba teaches the claimed method of making a memory module comprising: attaching at least one memory integrated circuit to a printed circuit board (semiconductor memory 1; Fig. 2,3), said printed

circuit board comprising data bus contacts on a portion thereof (data bus 21; Fig. 3; 4/43-50; 5/47-63); coupling said data bus contacts on said printed circuit board to data bus terminals on said memory integrated circuit through a bus switch (switching circuit 26; Fig. 2,3; 4/43-55; 5/47-63); and interfacing a state decoder (bus line switching circuit 20) with a memory controller (controller 24), wherein the state decoder selectively controls the bus switch to reduce data capacitance (Fig. 3; 4/43-55; 5/47-63; effect/result of bus switching).

9. Wiggers a memory system and method for reducing memory capacitance. Wiggers teaches the claimed method of making a memory module comprising: attaching at least one memory integrated circuit to a printed circuit board (semiconductor memory 22; Fig. 3,4), said printed circuit board comprising data bus contacts on a portion thereof (data bus 23; Fig. 3; 4/44-50); coupling said data bus contacts on said printed circuit board to data bus terminals on said memory integrated circuit through a bus switch (switches 29; Fig. 3,4; 4/44-6/11); and interfacing a state decoder (memory controller 21) with a memory controller (main board 25), wherein the state decoder selectively controls the bus switch to reduce data capacitance (4/25-30,53-60).

As to claim 3,7:

10. Baba teaches interfacing a state decoder with the bus switch (control circuit 6,24; Fig. 2,3).

11. Wiggers teaches interfacing a state decoder with the bus switch (control terminal 37; Fig. 4; 5/40-50).

As to claim 4,8:

12. Baba teaches the state decoder is structured to decode at least one control gate and control the bus switch in response thereto (the control circuit controls the bus switch 5; 5/1-10; 6/50-60).

13. Wiggers teaches the state decoder is structured to decode at least one control gate and control the bus switch in response thereto (control terminal controls the bus switch; 5/40-50).

As to claim 10:

14. Baba teaches the bus switch is external to the memory integrated circuit (Fig. 2,3).

15. Wiggers teaches the bus switch is external to the memory integrated circuit (Fig. 4)

As to claim 11:

16. Baba teaches the method of making a memory integrated circuit comprising the acts of: connecting data input terminals to an input portion of a bus switch; connecting an output portion of said bus switch to a data input buffer; and coupling an output of said data input buffer to a memory storage circuit (Fig. 2,3); and interfacing a state decoder (bus line switching circuit 20) with a memory controller (controller 24), wherein the state decoder selectively controls the bus switch to reduce data capacitance (Fig. 3; 4/43-55; 5/47-63; effect/result of bus switching).

17. Wiggers teaches the method of making a memory integrated circuit comprising the acts of: connecting data input terminals to an input portion of a bus switch; connecting an output portion of said bus switch to a data input buffer; coupling an output of said data input buffer to a memory storage circuit (Fig. 4); and interfacing a state decoder (memory controller 21) with a memory controller (main board 25), wherein the state decoder selectively controls the bus switch to reduce data capacitance (4/25-30,53-60).

As to claim 13:

18. Baba teaches the bus switch electrically removes a portion of the data bus associated with unaccessed memory circuits (only use nondefective/unaccessed circuit 5/1-10).

19. Wiggers teaches the bus switch electrically removes a portion of the data bus associated with unaccessed memory circuits (decouple bus when memory is not used/accessed; 6/5-10)

As to claim 14:

20. Wiggers teaches capacitance of the memory circuits is associated with the data bus (6/5-11).

As to claim 15:

21. Baba teaches the memory integrated circuit comprises the bus switch 26 (Fig. 3)

22. Wiggers teaches the memory integrated circuit comprises the bus switch 29 (Fig. 3)

As to claim 16,17:

23. Baba teaches the memory integrated circuit comprises the state decoder (control 24; Fig. 3)

24. Wiggers teaches the memory integrated circuit comprises the state decoder (memory controller 21; Fig .3)

As to claim 18:

25. Baba teaches the state decoder is located within the memory integrated circuit (control 24; Fig 3).

26. Wiggers teaches the state decoder is located within the memory integrated circuit (controller 21; Fig. 3)

As to claim 19:

27. Baba teaches the bus switch is located within the memory integrated circuit (switch 26; Fig. 3)

28. Wiggers teaches the bus switch is located within the memory integrated circuit (switch 29; Fig .3)

As to claim 20:

29. Baba teaches interfacing the state decoder with the bus switch (control 24 is connected/interfaced with circuit 20).

30. Wiggers teaches interfacing the state decoder with the bus switch (controller 21 is interfaced with board 25).

As to claim 21:

31. Baba teaches the state decoder is structured to decode at least one control gate and control the bus switch (controller 24 controlled by address signal; 5/47-62).

32. Wiggers teaches the state decoder is structured to decode at least one control gate and control the bus switch (controller is controlled by control signal line; 4/50-605/52-67)

Claim Rejections - 35 USC § 103

33. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

34. Claims 2,6,9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Baba (US 5,303,192) OR Wiggers (US 6,011,710).

As to claim 2,6:

35. Baba does not specifically teach the memory integrated circuit comprises synchronous DRAM but does teaches the memory may be formed by other memory elements such as DRAM/SRAM such as SRAM (10/35-40). It is well-known in the art at the time of the invention was made that SDRAM is a common substitute for DRAM/SRAM, depending on the application. Thus, it would have been obvious to one of ordinary skills in the art to substitute another memory, such as SDRAM, for the DRAM/SRAM of Baba, as suggested by Baba.

36. Wiggers does not specifically teach the memory integrated circuit comprises synchronous DRAM but does teaches the memory may be formed by other memory elements such as ROM, DRAM, or RAM (4/50-54). It is well-known in the art at the time of the invention was made that SDRAM is a common substitute for DRAM/RAM, depending on the application. Thus, it would have been obvious to one of ordinary skills in the art to substitute another memory, such as SDRAM, for the DRAM/RAM of Wiggers, as suggested by Wiggers.

As to claim 9:

37. Baba does not specifically teach the memory integrated circuit comprises the switch. It has been found by the court that combining several elements together as an integral unit is a matter of obvious engineering choice, and would be obvious to one of ordinary skills in the art (In re Larson, 340 F.2d 965, 968, USPQ 347, 349 (CCPA 1965)).

38. Wiggers does not specifically teach the memory integrated circuit comprises the switch. It has been found by the court that combining several elements together as an integral unit is a matter of obvious engineering choice, and would be obvious to one of ordinary skills in the art (In re Larson, 340 F.2d 965, 968, USPQ 347, 349 (CCPA 1965)).

Conclusion

39. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Than Nguyen whose telephone number is 571-272-4198. The examiner can normally be reached on 8am-3pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571)272-4201. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Than Nguyen
Examiner
Art Unit 2187